REMARKS

Claims 1 - 14 remain pending in the present application, of which claims 4 - 11 have been withdrawn from consideration. By this Amendment, claims 1, 3, 12 and 14 have been amended. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **April 30, 2003**.

Claim Objections

Claims 1, 3 and 12 stand objected to on page 2 of the Action due to minor informalities. It is respectfully submitted that claims 1, 3 and 12 have been amended to correct such minor informalities. Accordingly, withdrawal of this objection is respectfully solicited.

Claim Rejection Under 35 USC 102(b)

Claim 14 stands rejected under 35 U.S.C. 102(b) as being anticipated by Park (USPN 5,770,877).

This rejection is respectfully traversed.

According to amended claim 14, the tunneling insulation film has a thickness enough to transmit carriers therethrough by a direct tunneling phenomenon. In contrast, Park's tunneling insulation film has a thickness enough to transmit carriers therethrough by a Fowler-Nordheim tunneling phenomenon as the Examiner confesses in the Office Action (page 3, lines 3 - 4).

Therefore, Park does not disclose the tunneling insulation film has a thickness enough to transmit carriers therethrough by a direct tunneling phenomenon.

Claim Rejection Under 35 USC 103(a)

Claims 1, 3, 12 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Hu et al. (USPN 5,511,030).

Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Hu and Shigyo (USPN 6,222,224).

Both of these rejections are respectfully traversed.

The Examiner states that it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the memory device of Park having a thin direct tunneling insulating film as taught by Hu. Applicants take issue with the Examiner's statement.

Park states that electrons accumulated in the floating gate F.G. are induced to a source S via a thin gate oxide layer (electrons are emitted from the floating gate) and erasure is continued in the prior art (column 2, lines 36-46). According to Park's invention, the floating gate (13) is

apart from the source (14) as shown in FIG 9. As a result, electrons accumulated in the floating gate (13) can be prevented from being induced to the source (14) and being emitted.

// no [illegible] request interview agreed not accept!

Hu states that such a PNVM cell has a data retention period substantially less than ten years because the direct tunneling dielectric allows greater charge leakage (column 3, lines 13-15). If Park's tunneling insulation film (16) is replaced by Hu's direct tunneling insulation dielectric (102), charge leakage from the floating gate (13) to the substrate 10 must become greater. Increase of the charge leakage contradicts the advantageous effect of Park's invention to prevent electrons accumulated in the floating gate from being emitted.

// no support

Therefore, it would not have been obvious to modify the memory device of Park having a thin direct tunneling insulating film as taught by Hu.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE
U.S. SERIAL NO. 09/726,386

IN THE CLAIMS:

Claims 1, 3, 12 and 14 have been amended to read as follows:

1. (Twice Amended) A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a direct tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the direct tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode.

3. (Amended) A semiconductor memory according to claim 1, further comprising:

a dielectric film formed on an upper surface of said floating gate electrode, said dielectric film having a thickness not allowing carriers to transmit therethrough by the <u>direct</u> tunneling phenomenon; and

a second control gate electrode formed on said dielectric film and electrically connected to said first control gate electrode, said second control gate electrode and said floating gate electrode constituting a capacitor,

wherein said first control gate electrode is formed on said gate insulating film also over a side wall of said second control gate electrode.

12. (Amended) A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness of at most 3nm;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by [the] <u>a direct</u> tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode.

14. (Amended) A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a <u>direct</u> tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the <u>direct</u> tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode,

wherein a surface layer of said semiconductor substrate under said first control gate electrode has a conductivity opposite to that of said impurity doped regions.